0-7 inputs of all the chips are also tied together. A specific example of two cascaded chips illustrates the technique (FIG. 8). Timing (FIG. 9) is similar to the sample 4-tap FIR, except the $\overline{\text{ERASE}}$ and $\overline{\text{SENBL}}$/$\overline{\text{SENBH}}$ signals must be enabled independently for the two DFP chips in order to clear the correct accumulators and enable the SUM 0-25 output signals at the proper times.

SINGLE CHIP CONFIGURATION

Using a single DFP chip, a filter of length k>4 can be constructed by processing in k/4 passes as illustrated in the table shown in FIG. 10 for an 8-tap FIR. Each pass is composed of $Tp=3+k+Td$ cycles and computes 4 output samples. In pass i, the samples with indexes (i−1)*4+1 to i*4 enter the DIN 0-7 inputs. The coefficients Cl-Ck enter the CIN 0-7 inputs, followed by 3 zeros. As these zeros are entered, the result samples are output and the accumulators reset. Initial filling of the pipeline is not shown in this sequence table. Filter outputs can be put through a FIFO to even out the sample rate.

EXTENDED COEFFICIENT AND DATA SAMPLE WORD SIZE

The sample and coefficient word size can be extended by utilizing several DFP chips in parallel to get the maximum sample rate or a single chip with resulting lower sample rates. The technique is to compute partial products of 8×8 and combine these partial products by shifting and adding to obtain the final result. The shifting and adding can be accomplished with external adders (for full speed) or with the DFP's shift and add mechanism contained in its output stage (at reduced speed).

Before discussing these techniques, appropriate notation must be established. Consider the multiplication of two 16-bit numbers. Let

$$C=C_M+C_L$$

where

C_M=most significant byte,
C_L=least significant byte

$$X=X_M+X_L$$

where

X_M=most significant byte
X_L=least significant byte

Then

$$C\times X=(C_M+C_L)\times(X_M+X_L))=C_{M\times XM}+C_L\times X\text{-}M+C_M\times X_L+C_L\times X_L.$$

The partial product bits line up as follows:

15	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
$C_M \times X_M$	• • • • • • • • • • • • • • • •	
$C_L \times X_M$	• • • • • • • • • • • • • • • •	
$C_M \times X_L$	• • • • • • • • • • • • • • • •	
$C_L \times X_L$	• • • • • • • • • • • • • • • •	

MULTIPLE DFP WORD SIZE EXTENSION

A fourth order FIR with 16-bit coefficients and data and 20 MHz sample rate can be constructed with four DFP chips 10 and three external adders 44 (FIG. 11). Different 8×8 partial products are accumulated in each DFP chip at a 20 MHz rate and combined by the external adders to form the result. The least portions (X_L and C_L) are in unsigned mode.

SINGLE DFP WORD SIZE EXTENSION

A single 4-tap DFP can multiply word sizes up to n×32 bits with any number of bits. A single 4 tap DFP may be used, for example to implement 24×16 MAC or 8×32 MAC. The technique can be illustrated by the sample of a 16×16 multiplication.

Using the partial product notation above, consider the multiplication of two 16×16 numbers. Three MAC cells are used to accumulate three overlapping partial products. CELL 0 accumulates the LSBs, CELL1 the middle bits and CELL2 the MSBs. Finally the partial products are combined using the shift and add capabilities of the output stage. CELL 0 operates in unsigned mode. CELL1 is MIXED mode and CELL2 is two's complement mode.

The 16-bit operands are input one byte at a time in the sequence shown in FIG. 12. Detailed timing of 16×16 multiplication, including pipelining, is shown in FIG. 13.

DECIMATION/RESAMPLING

A useful function in many digital signal processing systems is sample rate reduction or decimation. Prior to decimation the signal must be low pass filtered to prevent aliasing when the sample rate is reduced. If, for example, decimation by a factor of 2 is desired, only every other output of the low pass filter is used. If only the needed outputs are calculated, the processing requirements are halved. FIR filters are particularly convenient for decimation since their output depends only on present and past inputs and not on past outputs.

The DFP of FIG. 2 provides a mechanism for decimating by factors of 2, 3 or 4. From the DFP filter cell block diagram (FIG. 3), note the three D registers 18 and two multiplexers 19 in the coefficient path through the cell. These allow the coefficients to be delayed by 1, 2, or 3 clocks through the cell. The sequence table (FIG. 14) for a decimate-by-two filter illustrates the technique (internal cell pipelining ignored for simplicity):

Detailed timing for a 20 MHz input sample rate, 10 MHz output sample rate (i.e. decimate-by-two), 8-tap FIR filter, including pipelining, is shown in FIG. 15.

IMAGE CORRELATION WITH THE DFP

The decimation registers can be used to provide a 3×3 or 4×4 correlation with one DFP device (FIG. 16). In the 4×4 application for example, the 16 kernel coefficients are stored properly interleaved within the decimation registers and recycled as the DFP is clocked. The image pixels are entered in column-scanned order into the DFP data input. Each DFP MAC cell accumulates the correlation sum for a single image point. Four points are being accumulated simultaneously, but overlapped. Once the pipeline is full, a